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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,856	11/08/2001	Hiroshi Suetsugu	NEC 01FN049	5048

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EXAMINER	
KOVALICK, VINCENT E	

ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 11/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/008,856	SUETSUGU ET AL.	
	Examiner	Art Unit	
	Vincent E Kovalick	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-15* is/are allowed.

6)☒ Claim(s) *1 and 3-8* is/are rejected.

7)☒ Claim(s) *2* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to Applicant's Amendment B Rule 116 with Submission of Priority Document dated August 24, 2004 in response to USPTO Final Action dated May 24, 2004.

Applicant's remarks relative to the rejection of claims 1 and 3-8, wherein the priority date (November 8, 2000) of the application precedes the priority date (August 17, 2001) of Hsu et al. (USP 6,674,417) reference used in the rejection of claims 1 and 3-8, are rendered moot with the introduction of Endo et al. (USP 5,107,176) prior art with a File Date of December 29, 1989. The said Endo prior art teaches an external power supply driving a plasma display, and replaces the Hsu et al. prior art initially used in the rejection of claims 1 and 3-8.

USPTO Final Office Action dated May 24, 2004 is herewith withdrawn.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (herein APA) taken with Endo et al. (USP 5,107,176).

Relative to claim 1, the Admitted Prior Art **teaches** a plasma display module; an interface board;

a plasma display panel; driving circuits which drive said plasma display panel; and a power circuit into which a external alternating current is inputted, said power circuit supplying driving voltages to said driving circuits; and a control voltage for controlling operation of said interface board, and operations of said power circuit being controlled with control signals output by said interface boards (Application disclosure, page 1, lines 11-17 and Prior Art Fig. 1).

Prior Art **does not teach** an external power circuit, wherein the source voltages of said interface board are supplied from said external power circuit, and outputting an external source voltage to be used by said external power circuit.

APA **teaches** a plasma display module comprising a power circuit, receiving an external AC input, said circuit for driving a plasma display module, said module including a interface board for system control and signal distribution.

Endo et al. **teaches** a Plasma Display Device (col. 2, lines 60-67; col. 3, lines 1-67 and col. 3, lines 1-39); Endo et al. further **teaches** an external power circuit, wherein the source voltages of said interface board are supplied from said external power circuit, and outputting an external source voltage to be used by said external power circuit (col. 1, lines 47-67; col. 2, lines 1-2 and Abstract).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by the APA the feature as taught by Endo et al. in order to provide a driving method for a plasma display unit which can effectively drive a plasma display unit by providing sufficient current for the plasma display to function.

4. Claims 3-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over APA taken with Endo et al. as applied to claim 1 in item 3 hereinabove, and further in view of Okada et al. (USP 5,5686,933).

Relative to claims 3-8, APA taken with Endo et al. **does not teach** said power circuits that: a) starts up a lowest-value voltage of said plurality of voltages earlier than a highest-value voltage of said plurality of voltages; b) shuts down a highest-value voltage of said plurality of voltages earlier than a lowest-value voltage of aid plurality of voltages; or c) starts-up a lowest-value voltage of said plurality of voltages earlier than a highest-value voltage of said plurality of voltages and shuts down said highest-value voltage earlier than said lowest-value voltage.

APA taken with Endo et al. teaches a plasma display module comprising a power circuit, receiving an AC input, said circuit for driving a plasma display module, said module including an interface board for system control and signal distribution, and an external power for receiving an input from the system power circuit and generating a multiple voltage input signal to the said interface board.

APA taken with Endo teaches an plasma display device powered from an external power source.

Okada et al. **teaches** a driving circuit for a display apparatus (col. 2, lines 46-67; col. 3,lines 12-67 and col. 4, lines 1-24); Okada et al. further **teaches** the means to regulate said power circuits that a) starts up a lowest-value voltage of said plurality of voltages earlier than a highest-value voltage of said plurality of voltages; b) shuts down a highest-value voltage of said plurality of voltages earlier than a lowest-value voltage of aid plurality of voltages; and c) starts-up a lowest-value voltage of said plurality of voltages earlier than a highest-value voltage of said

plurality of voltages and shuts down said highest-value voltage earlier than said lowest-value voltage (col. 1, lines 9-17; col. 17, lines 37-41 and col. 18, lines 51-67 and col. 19, lines 1-3).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to supply to the devices as taught by APA taken with Endo et al. the feature as taught by Okada et al. in order to provide the means to sequence the voltages and related timing signals that drive the system display through the various states of start-up, display image, shut-down etc. and further control the desired image contrast (col. 4, lines 14-24, Okada et al.)

Allowable Subject Matter

5. Claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 2 the major difference between the teachings or the prior art of record (Endo et al. USP 5,107,176 and Okada et al., USP 5,686,933,) and that of the instant invention is that said prior art of record **does not teach** said plasma display module wherein control signals output by said interface board contain first and second control signals, and said power circuit outputs said control voltage to said interface board when an external alternating current is inputted to said power circuit, outputs said external power voltage to said external power circuit when said first control signal is inputted to said power circuit, and outputs said driving voltages to said driving circuits when said second control signal is inputted to said power circuit.

6. Claims 9-15 are allowed.

7. The following is an examiner's statement of reasons for allowance:

Relative to claim 9, the major difference between the teachings or the said prior art of record and that of the instant invention, is that said prior art of record **does not teach** said plasma display module wherein control signals output by said interface board contain first and second control signals, and said power circuit outputs said control voltage to said interface board when an external alternating current is inputted to said power circuit, outputs said external power voltage to said external power circuit when said first control signal is inputted to said power circuit, and outputs said driving voltages to said driving circuits when said second control signal is inputted to said power circuit.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U. S. Patent No.	6,448,947	Nagai
U. S. Patent No.	6,124,840	Kwon
U. S. Patent No.	6,040,827	Shiina et al.
U. S. Patent No.	4,027,195	Shutoh et al.

Responses

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent E Kovalick whose telephone number is 703 306-3020. The examiner can normally be reached on Monday-Thursday 7:30- 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703 305-4938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent E. Kovalick
November 8, 2004

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